IN THE CLAIMS

1. (Currently amended) A configurable circuit arrangement comprising at least one circuit component at which a load is applied that can vary during operation of said circuit arrangement, wherein said configurable circuit arrangement comprises:

a. load determination means for determining a load applied at said at least one configurable circuit component having different fan-in or fan-out depending on a configuration of said circuit arrangement; and

b. adjusting means for, responsive to said determination means, adjusting drive capacity of said at least one circuit component to a value less than a maximum drive capacity while still meeting a delay specification~~responsive to said determination means~~.

2. (Previously presented) A circuit arrangement according to claim 1, wherein said determination means is configured to determine said load based on a configuration information loaded to said circuit arrangement.

3. (Previously presented) A circuit arrangement according to claim 2, wherein said configuration information is stored in a configuration memory.

4. (Previously presented) A circuit arrangement according to claim 2, wherein said configuration information comprises a configuration bit stream defining at least one of an input load and an output load of said at least one component.

5. (Previously presented) A circuit arrangement according to claim 1, wherein said

adjusting means is configured to vary a buffer or a buffer number of said at least one component.

6. (Previously presented) A circuit arrangement according to claim 5, wherein said adjusting means is configured to switch on or off buffers or buffer sections responsive to said determination means.

7. (Previously presented) A circuit arrangement according to claim 5, wherein said adjusting means is adapted to generate at least one control signal for switching on or off said buffer sections.

8. (Currently amended) A circuit arrangement according to claim 6, wherein said adjusting means is adapted to derive said control signal only from a most significant bit signal of a selection signal obtained from said determination means ~~50~~.

9. (Previously presented) A circuit arrangement according to claim 1, wherein said adjusting means is configured to vary a threshold voltage of circuit elements of said circuit arrangement.

10. (Previously presented) A circuit arrangement according to claim 9, wherein said adjusting means is adapted to change at least one bias voltage responsive to said determination means.

11. (Previously presented) A circuit arrangement according to claim 1, wherein said circuit arrangement is a field programmable gate array device.

12. (Currently amended) A method of controlling power consumption of a configurable circuit arrangement, said method comprising the steps of:

a. determining a load applied at at least one circuit component having different fan-in or fan-out depending on a configuration of said configurable circuit arrangement~~circuit arrangement~~; and

b. adjusting a drive capacity of said at least one circuit component responsive to said determination step to a value less than a maximum drive capacity while still meeting a delay requirement.